THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 51

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte VICTOR M. MORGANTI, PATRICK E. PRANGE, JAMES B. GEYER AND GEORGE J. BARLOW

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Appeal No. 94-3596
Application 07/689,655[1]

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ON BRIEF

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Before HARKCOM, Vice Chief Administrative Patent Judge, and HAIRSTON and FLEMING, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

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[1] Application for patent filed April 23, 1991. According to applicants, the application is a continuation of Application 07/311,363, filed February 13, 1989, abandoned; which is a continuation of Application 06/869,147, filed May 30, 1986, abandoned.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1 through 4 and 6 through 20. In an Amendment After Final[2] (paper number 41), claims 1, 4 and 7 were amended, and claim 3 was canceled. Accordingly, claims 1, 2, 4 and 6 through 20 remain before us on appeal.

The disclosed invention relates to a data processing system and method wherein a command instruction signal group generated in a first central processing unit is executed in a second central processing unit.

Claim 1 is illustrative of the claimed invention, and it reads as follows:

1. A data processing system wherein a command instruction signal group generated in a first central processing unit is executed in a second central processing unit, said data processing system comprising:

a system bus; and

a plurality of central processing units coupled to said system bus, said plurality of central processing units including a source central processing unit and a target central processing unit, said central processing units receiving signal groups from and applying signal groups to said system bus, each of said

[2] On page 7 of the amendment, appellants state that claim 6 is canceled by the amendment. Since the amendment never specifically requested the Office to cancel claim 6, it is still on appeal.

central processing units including;

execution apparatus for processing data signal groups in said each central processing unit in response to control signals resulting from decoding of instruction signal groups, wherein said source central processing unit includes condition apparatus for generating a command signal group in response to and determined by a preestablished condition in said source central processing unit, said command signal group being applied to said system bus along with a target central processing unit address signal group,

said target central processing unit including an interface means for identifying said target processing unit address signal group and for storing said command signal group applied to said system bus having said target processing unit address signal group;

said target central processing unit including decode logic coupled to at least one preselected component of said second central processing unit execution apparatus, said decode logic decoding said stored command signal group, said decode logic applying control signals resulting from said decoding to said preselected component of said target central processing unit thereby executing said command signal group without software intervention, wherein storing said command signal group in said target central processing unit suspends execution by said execution apparatus of said target central processing unit of a currently executing instruction signal group sequence upon completion of a currently executing instruction signal group, wherein said control signals are applied to said preselected component upon completion of execution of said currently executing instruction signal group.

The references relied on by the examiner are:

Gunter et al. (Gunter)	4,349,873	Sep. 14, 1982
Vrielink et al. (Vrielink)	4,482,954	Nov. 13, 1984
Vince	4,562,539	Dec. 31, 1985
Bomba et al. (Bomba)	4,648,030	Mar. 3, 1987 (filed Sep. 22, 1983)

Claims 1, 2, 4, 6 through 11, 13, 14, 16, 17 and 20 stand

rejected under 35 U.S.C. § 103 as being unpatentable over Vince in view of Bomba.

Claims 12, 18 and 19 stand rejected under 35 U.S.C. § 103 as being unpatentable over Vince in view of Bomba and Vrielink.

Claim 15 stands rejected under 35 U.S.C. § 103 as being unpatentable over Vince in view of Bomba and Gunter.

Reference is made to the final rejection, the briefs and the answer for the respective positions of the appellants and the examiner.

OPINION

We have carefully considered the entire record before us, and we will reverse the obviousness rejection of claims 1, 2, 4 and 6 through 20.

In the claims on appeal, a first (i.e., source) central processing unit generates a command signal group that is stored in a second (i.e., target) central processing unit. The storage of the command signal group in the second central processing unit causes a suspension of instruction signal group execution upon completion of a currently executing instruction signal group.

Vince discloses a data processing system (Figure 1) that has a plurality of data processing units or nodes 10. Each of the data processing units 10 has access to shared data common to two

or more of the data processing units 10 via data couplers 12 and communication link 11. Figure 2 of Vince is a diagram of one of the data processing units 10. When the processor 14 in the data processing unit updates a shared data item, a message containing the updated value of the data item and its address is generated and is transmitted via output buffer 18 and the link 11 to the other data processing units 10 (column 1, lines 58 through 64). When the message is received by the other data processing units, it is used to update the copies of the shared data item held in the stores of those data processing units to thereby ensure that all copies of the shared data item are kept consistent (column 1, lines 65 through 68). The operation of a data processing unit that transmits an update message on the link is suspended if it receives an update message from another data processing unit while there are one or more update messages still outstanding from the transmitting data processing unit (column 5, lines 57 through 60). The operation of the transmitting data processing unit is suspended because the received message may overwrite a data item which has already been updated by the transmitting data processing unit at the time it created the outstanding data message. Without the suspension in operation, a data item may be overwritten by a chronologically earlier data value (column 5,

lines 29 through 36).

During normal operation of Vince's data processing system, a message update is stored in the data processing unit without any suspension of operation of the data processor contained therein. If a data processing unit has one or more outstanding update messages, and in the interim receives an update massage from another data processing unit, then the data processing unit with the one or more outstanding update messages will make a local decision to suspend operation of the data processor contained therein. The local command in Vince to suspend operation of the data processor contrasts with the claimed remote source command to suspend operation of a target processor. Thus, we agree with appellants' argument (Brief, pages 19 through 21, and Reply Brief, page 5) that the suspension of operation for the specified condition in Vince is not analogous to the claimed suspension of instruction execution in the target processor.

Figure 1C of Bomba operates as follows:

> In accordance with the present invention, therefore, the first device [50] also includes means for selectively registering accesses of the local memory [54] that have occurred by way of the common communications path [68] and may thus have resulted in caching of the local-memory contents involved in the access. When the first device [50] uses its private communications path [58] to write to a local-memory [54] location that has been involved in such an access, the first device [50] sends the invalidate command over

> the common path [68] so that devices [52] having cache memories [190] can set flags to invalidate associated cache-memory locations. In this way, devices [52] having cache memories [190] can keep track of whether their cache data are valid or invalid even when the local memory [54] is accessed by way of the private communications path [58] (column 4, lines 45 through 59).

The invalidation teachings of Bomba are not relevant to the claimed suspension of instruction execution in a target processor.

The obviousness rejection of claims 1, 2, 4, 6 through 11, 13, 14, 16, 17 and 20 is reversed because neither Vince nor Bomba teaches or would have suggested the claimed suspension operation.

The obviousness rejection of claims 12, 15, 18 and 19 is reversed because the teachings found in Vrielink and Gunter do not cure the noted shortcomings in the teachings of Vince and Bomba.

DECISION

The decision of the examiner rejecting claims 1, 2, 4 and 6 through 20 under 35 U.S.C. § 103 is reversed.

REVERSED

GARY V. HARKCOM, Vice Chief Administrative Patent Judge	)	
KENNETH W. HAIRSTON Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
MICHAEL R. FLEMING Administrative Patent Judge	)	

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